What is claimed is:

1. A method of testing memory, comprising:

providing one or more semiconductor wafers having one or more semiconductor chips thereon, each said chip comprising one or more segments, each said segment comprising one or more memory cells;

providing a programmable testing apparatus comprising one or more test pattern generators and a test bed adapted to receive said one or more wafers in communicative contact so as to address individual memory cells, segments, chips, and wafers and transmit information thereto and receive information therefrom;

receiving one or more test commands;

constructing a test sequence of one or more commanded tests from said test commands;

constructing at least one header comprising location information for each said wafer, chip, segment, and memory cell;

testing said memory cells with one or more test patterns generated by said test pattern generator;

collecting the results of said testing and passing them to a display device;

passing said location information to said display device;

constructing and displaying a graphical representation of said test results using said location information.

2. The method of claim 1 wherein a header is constructed for each commanded test.

3. The method of claim 1 wherein said graphical representation comprises a wafer display comprising a plurality of first graphical objects, each representing a chip, arranged spatially in accordance with the physical location of each said chip on said wafer.

4. The method of claim 3 wherein said wafer display further comprises an indication of failed chips.

5. The method of claim 3 wherein said wafer display further comprises an indication of which chip is currently being tested.

6. The method of claim 3 wherein said wafer display further comprises an indication of which chips have been tested.

7. The method of claim 1 wherein said graphical representation further comprises a chip display comprising a plurality of second graphical objects, each representing a segment.

8. The method of claim 7 further comprising an indication of failed segments.

9. The method of claim 1 wherein said graphical representation further comprises a segment display comprising graphical objects for each segment within a chip and further comprising an indication of which segment is currently being tested.

10. The method of claim 1 wherein said graphical representation further comprises a segment information display comprising graphics for displaying detailed segment information and the locations of any failed memory cells.

11. A program storage device, readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for testing semiconductor memory, the method comprising:

providing one or more semiconductor wafers having one or more semiconductor chips thereon, each said chip comprising one or more segments, each said segment comprising one or more memory cells;

providing a programmable testing apparatus comprising one or more test pattern generators and a test bed adapted to receive said one or more wafers in communicative contact so as to address individual memory cells, segments, chips, and wafers and transmit information thereto and receive information therefrom;

receiving one or more test commands;

constructing a test sequence of one or more commanded tests from said test commands;

constructing at least one header comprising location information for each said wafer, chip, segment, and memory cell;

testing said memory cells with one or more test patterns generated by said test pattern generator;

collecting the results of said testing and passing them to a display device;

passing said location information to said display device;

constructing and displaying a graphical representation of said test results using said location information.

12. The apparatus of claim 12 wherein a header is constructed for each commanded test.

13. The apparatus of claim 12 wherein said graphical representation comprises a wafer display comprising a plurality of first graphical objects, each representing a chip, arranged spatially in accordance with the physical location of each said chip on said wafer.

14. The apparatus of claim 14 wherein said wafer display further comprises an indication of failed chips.

15. The apparatus of claim 14 wherein said wafer display further comprises an indication of which chip is currently being tested.

16. The apparatus of claim 14 wherein said wafer display further comprises an indication of which chips have been tested.

17. The apparatus of claim 12 wherein said graphical representation further comprises a chip display comprising a plurality of second graphical objects, each representing a segment.

18. The apparatus of claim 12 wherein said graphical representation further comprises a segment information display comprising graphics for displaying detailed segment information and the locations of any failed memory cells.

19. The apparatus of claim 17 wherein said chip display appears for any one chip when a user mouse-clicks on a corresponding said first graphical object.

20. The apparatus of claim 18 wherein said segment information display appears for any one segment when a user mouse-clicks on a corresponding said second graphical object.